CCD261-04 Back Illuminated AIMO Deep Depleted CCD Sensor

FEATURES

- Full Frame Spectroscopic Sensor
- 2048 by 264 Pixel Format
- 15µm Square Pixels
- Active image area 30.72 x 3.96 mm
- Deep Depleted for higher red response
- Advanced Inverted Mode Operation (AIMO)

INTRODUCTION

The CCD261-04 is a full frame spectroscopic format sensor product from Teledyne e2v.

The CCD261-04 has 2048(H) x 264(V) elements. Each element is 15 µm square. Standard three phase clocking and buried channel charge transfer are employed and Advanced Inverted Mode Operation (AIMO) is included as standard. Teledyne e2v's AIMO structure gives a 100 times reduction in dark current with minimum reduction in full well capacity. Novel Deep Depletion AIMO technology enhances IR sensitivity while preserving high spatial resolution and low dark current.

Designers are advised to consult Teledyne e2v should they be considering using CCD sensors in abnormal environments or if they require customised packaging or performance features.

TYPICAL PERFORMANCE

Pixel readout frequency	1 MHz
Output amplifier sensitivity	6.3 µV/e^-
Peak signal	75 ke^-/pixel
Spectral range	250–1050 nm

GENERAL DATA

Format

Active Image area	30.72 x 3.96 mm
Active pixels	2048 (H) x 264 (V)
Pixel size	15µm square
Number of output amplifiers	1

Package

Overall dimensions	35.5 x 20.0 mm
Number of pins	20
Inter-pin spacing	2.54 mm
Package type	Ceramic DIL

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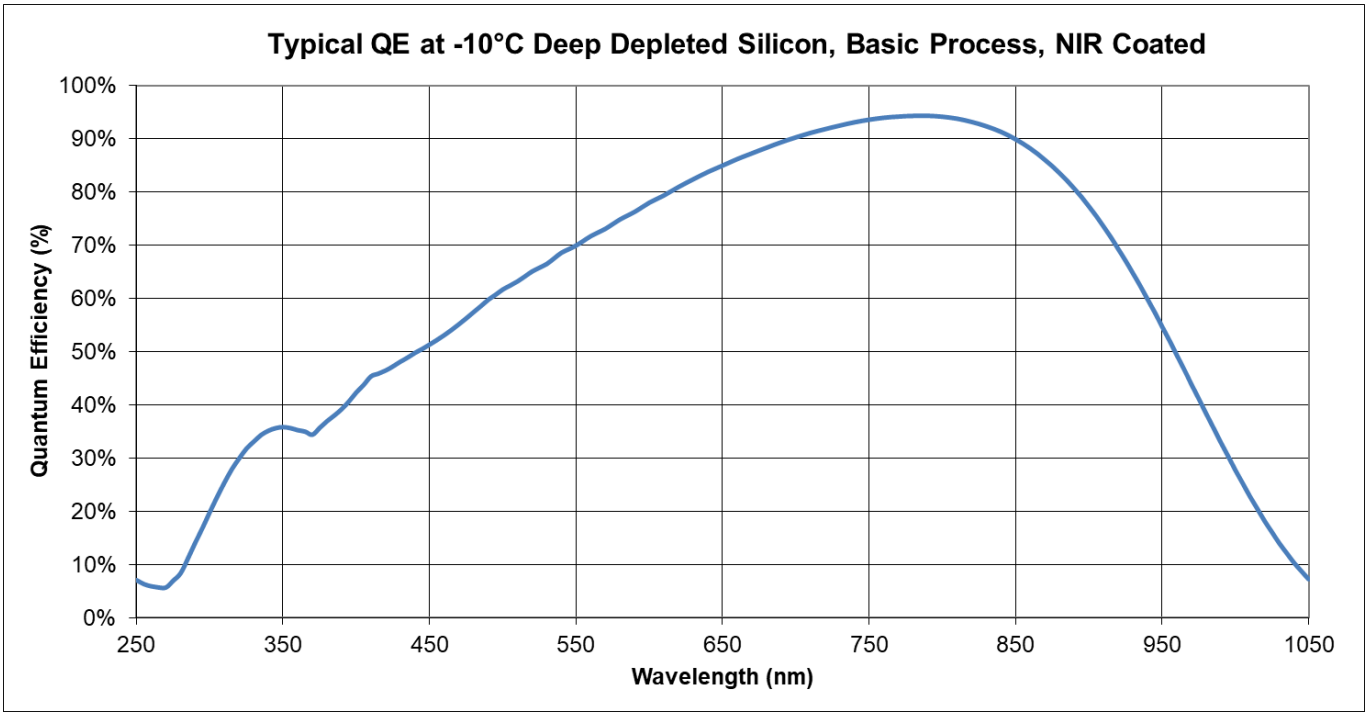
ELECTRO-OPTICAL PERFORMANCE (At 263K unless stated)

Parameters		Min	Typical	Max	Units	Notes
Output amplifier responsivity		5.5		7.8	μV/e-	Note 1
Image full well capacity			75		ke-/pixel	Note 2
Register full well capacity			650		ke-/pixel	Note 2
Output amplifier full well capacity			370		ke-	Note 2
Readout noise at 50kHz				4	e- rms	
Pixel readout frequency			1	3	MHz	Note 2, 3 & 4
QE	400nm	26			%	
	500nm	47			%	
	650nm	70			%	
	900nm	55			%	
Photo Response Non Uniformity	400nm			4	%	Note 5
	650nm			3	%	
	900nm			3	%	
Dark signal				45	e-/pix/s	Note 6
Binned Column Dark Signal non-uniformity (DSNU)				5	e-/pix/s	Note 7

NOTES

1) All tests are at a pixel rate of 500kHz, except the noise test.
2) These values are inferred by design and not measured.
3) The quoted maximum frequencies assume a 20pF load and that correlated double sampling is being used.
4) This max pixel rate limit refers to that set by the output amplifier.
5) Photo Response Non-Uniformity (PRNU) is defined as the local 1σ variation in photo response to flat field illumination. Any pixels classed as dark defects at high light level are omitted from the analysis.
6) The quoted dark signal has approximately the usual temperature dependence for inverted mode operation. There will also be a component generated during readout through the register, with non-inverted mode temperature dependence. Clock induced charge is only weakly temperature dependent, is independent of integration time, and depends on the operating biases and timings employed. It is typically 0.26 e^- / pixel/frame at T = - 10 °C. For more information, refer to the technical note "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors"
7) DSNU is defined as the 1σ variation of the dark signal.

TYPICAL SPECTRAL RESPONSE



COSMETIC SPECIFICATION

Maximum allowed defect levels are indicated below.

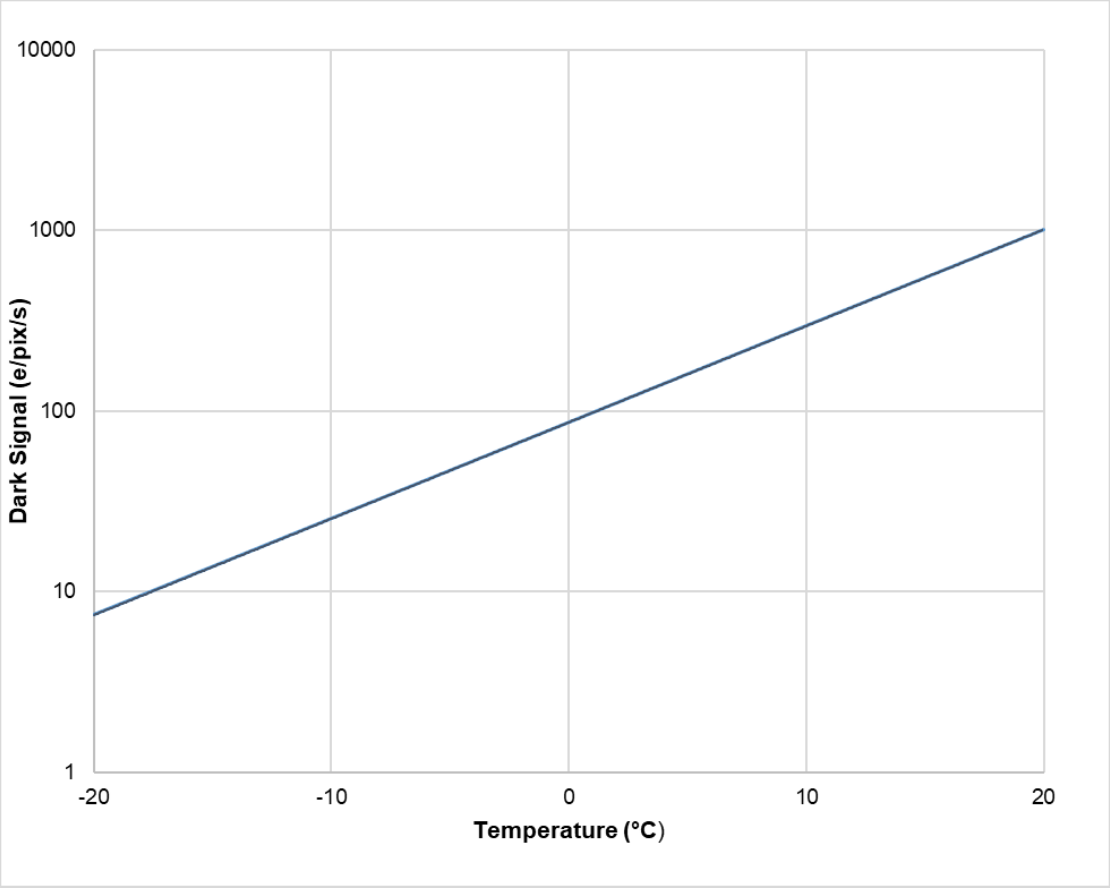
GRADE	1
White Column defects	1
Black Column defects	2
White spots	60
Black spots	60
Traps	4

Grade 5 devices are also available as electrical samples. These are confirmed to have working outputs and will nominally provide an image. Not all parameters are guaranteed to be tested or provided and the image quality may be worse than that of a grade 1.

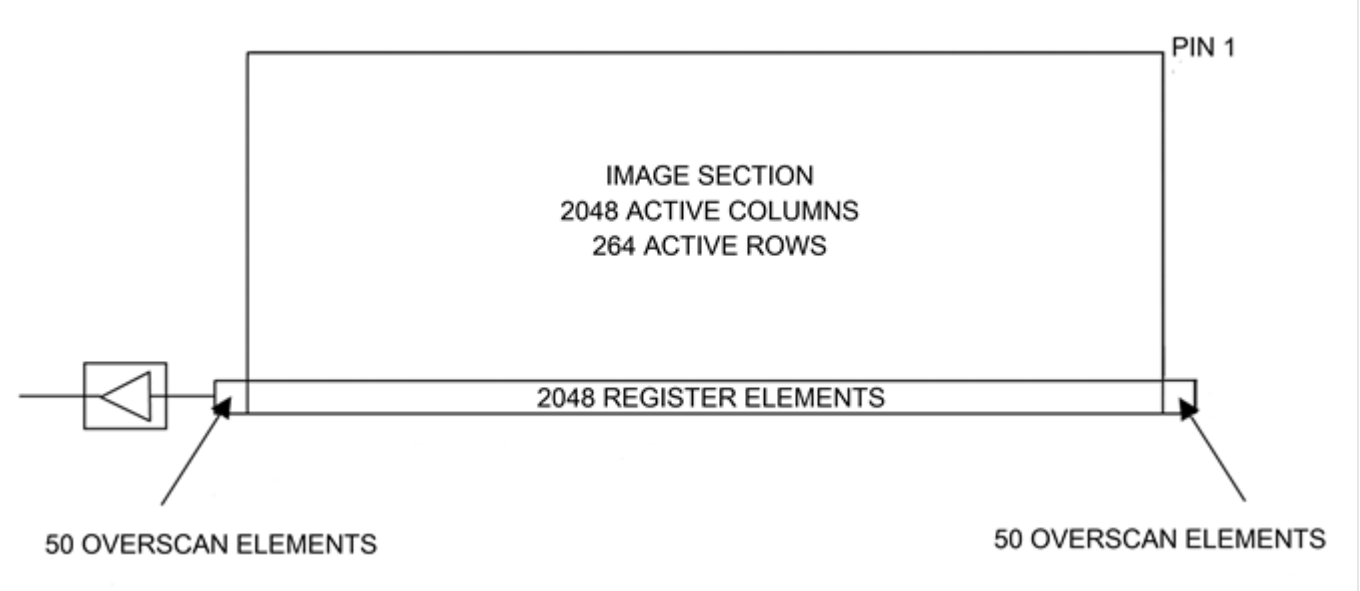
DEFINITIONS

White spots	A Bright Defect in Darkness is defined as any pixel whose mean response in darkness exceeds 100 times the specification for the maximum dark signal, at the test temperature.
Black spots	A dark defect at high light level is defined as any pixel whose mean photo response is less than 90% of the local mean at a signal level of approximately 50% of image full well capacity.
White Column defects	A Bright Columns in Darkness is defined as 9 or more consecutive pixels in any column, whose mean response in darkness exceeds 10 times the specification for the maximum dark signal at the test temperature.
Black Column defects	A dark column at high light level is defined as any column containing 9 or more (not necessarily consecutive) dark defects at high light level.
Traps	Pixels where charge is temporarily held. Traps are counted if they have a capacity greater than 500 e^- at 263 K.

TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE



DEVICE SCHEMATIC



Not all connections are shown.

ELECTRICAL INTERFACE

PIN	REF	DESCRIPTION	CLOCK AMPLITUDE OR DC LEVEL (V) (see note 8)			MAX RATINGS with respect to FSS	Notes
			Min	Typical	Max		
1	FSS	Front Substrate	+7	+7.5	+11	N/A	13
2	IØ3	Image Clock High	+12	+15	+16	±20	13
		Image Clock Low	-0.5	0	+0.5	±20	
3	IØ2	Image Clock High	+12	+15	+16	±20	13
		Image Clock Low	-0.5	0	+0.5	±20	
4	IØ1	Image Clock High	+12	+15	+16	±20	13
		Image Clock Low	-0.5	0	+0.5	±20	
5	BSS	Back Substrate	-	0	FSS		11, 13
6	ØR	Reset Clock High	+8	+12	+15	±20	9
		Reset Clock Low	-0.5	0	+1.5	±20	
7	RØ3	Register Clock High	+8	+12	+15	±20	
		Register Clock Low	-0.5	0	+1.5	±20	
8	RØ2	Register Clock High	+8	+12	+15	±20	
		Register Clock Low	-0.5	0	+1.5	±20	
9	RØ1	Register Clock High	+8	+12	+15	±20	
		Register Clock Low	-0.5	0	+1.5	±20	
10	N/C	Not Connected		-		N/A	
11	N/C	Not Connected		-		N/A	
12	OG	Output Gate	+1	+3	+5	±20	
13	OS	Output Source		N/A		-0.3 to +35	10
14	OD	Output Drain	+27	+31	+32	-0.3 to +35	
15	RD	Reset Drain	+15	+18	+19	-0.3 to +35	
16	FSS	Front Substrate	+7	+7.5	+11	N/A	13
17	SW	Summing Well Clock High	+8	+12	+15	±20	
		Summing Well Clock Low	-0.5	0	+1.5	±20	
18	GD	Guard Drain	+27	+30	+32	-0.3 to +35	12
19	SG	Spare Gate	0	0	+5	±20	
20	BSS	Back Substrate	-10	0	FSS	-25 to +0.3	11, 13

NOTES

8) All operating voltages are with respect to image clock low level (nominally 0V). To ensure correct device operation, the drive circuitry must be designed so that any value in the range Min to Max can be set.

9) ϕR high level is typically 1V above the high level of RØ1, RØ2 & RØ3.

10) See details of output circuit. Do not connect to voltage supply but use a ~5 mA current source or a ~5 kΩ external load. The quiescent voltage on OS is typically 5V more positive than that on RD. The current through these pins must not exceed 20 mA. Permanent damage may result if, in operation, OS experiences short circuit conditions.

11) Adjust to achieve full depletion, it should be noted that only very minimal study has been performed into the depletion depth, so this voltage has not been optimised. Ensure that it is initially equal to 0V at power up and then ramped between an upper limit of +FSS and a minimum (i.e. greatest negative) value where point spread function (or MTF) shows no further improvement or where the current in BSS increases to ~1µA. If this voltage is too large then some increase in white defects may be seen, and so there can be a trade-off between this effect and of optimum PSF.

12) May need to be adjusted in conjunction with BSS voltage to minimise leakage currents.

13) There is an interdependence between the FSS, BSS, image section voltages and line transfer time. If one of these parameters is changed then it is often required to change one of the others.

14) If all voltages are set to the 'typical' values, operation at or close to specification should be obtained. Some adjustment within the minimum – maximum range specified may be required to optimise performance.

POWER UP/POWER DOWN

When powering the device up or down it is critical that any specified maximum rating is not exceeded. This includes ensuring that reverse bias voltages cannot be momentarily applied.

The CCD has 2 substrate connections. The front substrate FSS for the output circuit is set to 0 V initially and then, after drain and gate biases have been applied, raised to the typical value for IMO devices to achieve low dark current. The back substrate BSS is applied to the back surface of the CCD. To get full depletion a low or negative potential is applied. A guard drain is designed to isolate front and back substrates.

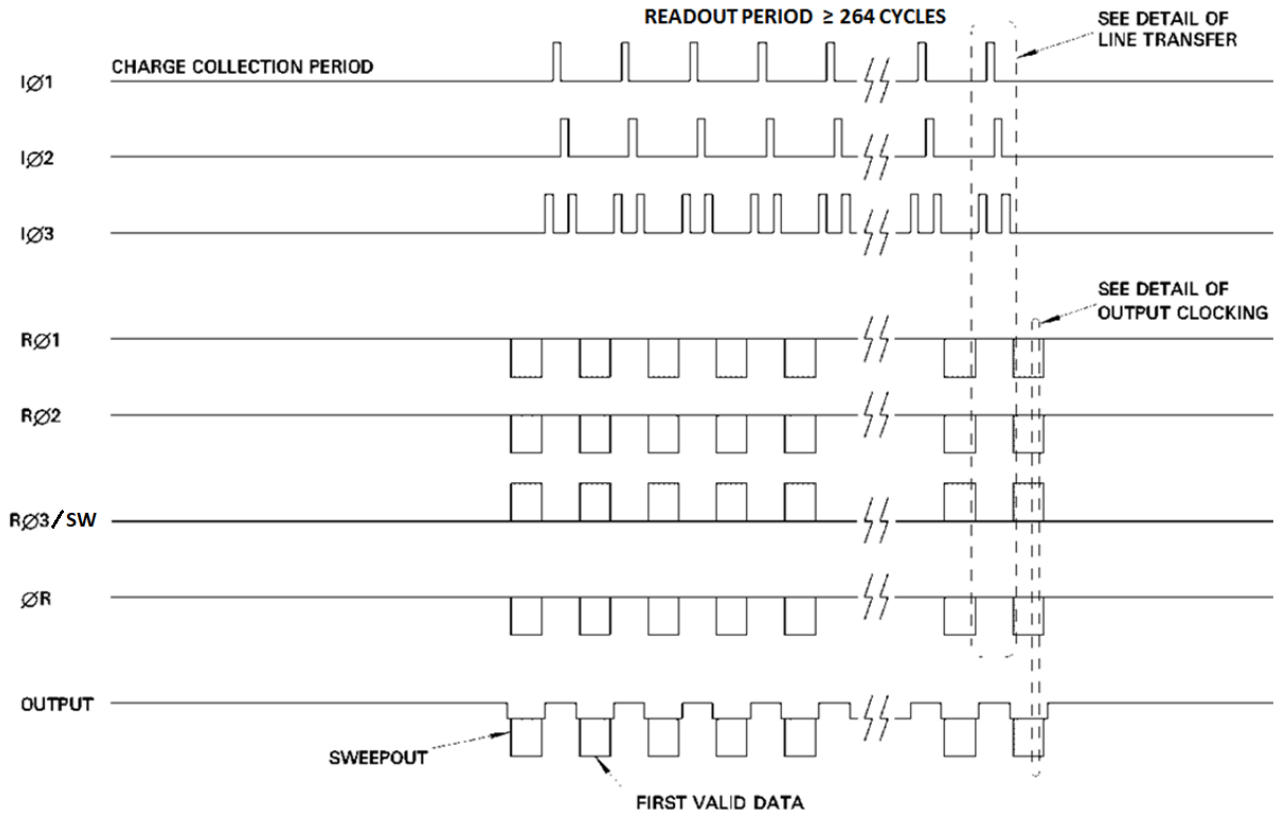
If there is a current flowing between FSS and BSS when switching on the guard drain, the insulation below the guard ring might not form properly. It is therefore advised to first set both FSS and BSS to 0V, then switch on the guard drain and all other biases and clocks in the order stated below, before applying any negative bias to BSS. The recommended power up order of all biases and clocks is listed in the table below.

BIAS/CLOCK	LABEL	POWER UP ORDER	Comment
Front Substrate	FSS	1	**Set to 0V at this stage**
Back Substrate	BSS	1	**Set to 0V at this stage**
Guard Drain	GD	2	
Reset Drain	RD	2	
Output Drain	OD	2	
Output Gate	OG	3	
Image Clock High	IØH	4	
Image Clock Low	IØL	4	
Register Clock High	RØH	4	
Register Clock Low	RØL	4	
Reset Gate High	ØRH	4	
Reset Gate Low	ØRL	4	
Front Substrate	FSS	5	**Set to desired voltage**
Back Substrate	BSS	6	**Set to desired voltage**

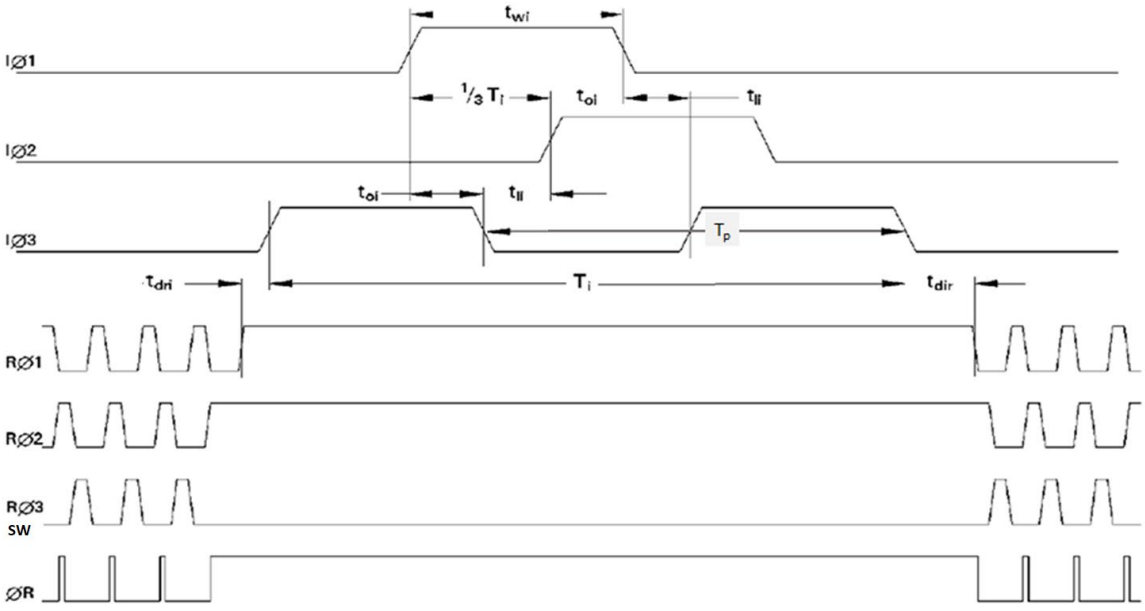
All levels must be settled before powering up the next group of biases. There can be a delay between the bias/clocks in any stated group.

It is also important to ensure that excess currents do not flow in the OS pins. Such currents could arise from rapid charging of a signal coupling capacitor or from an incorrectly biased DC-coupled preamplifier.

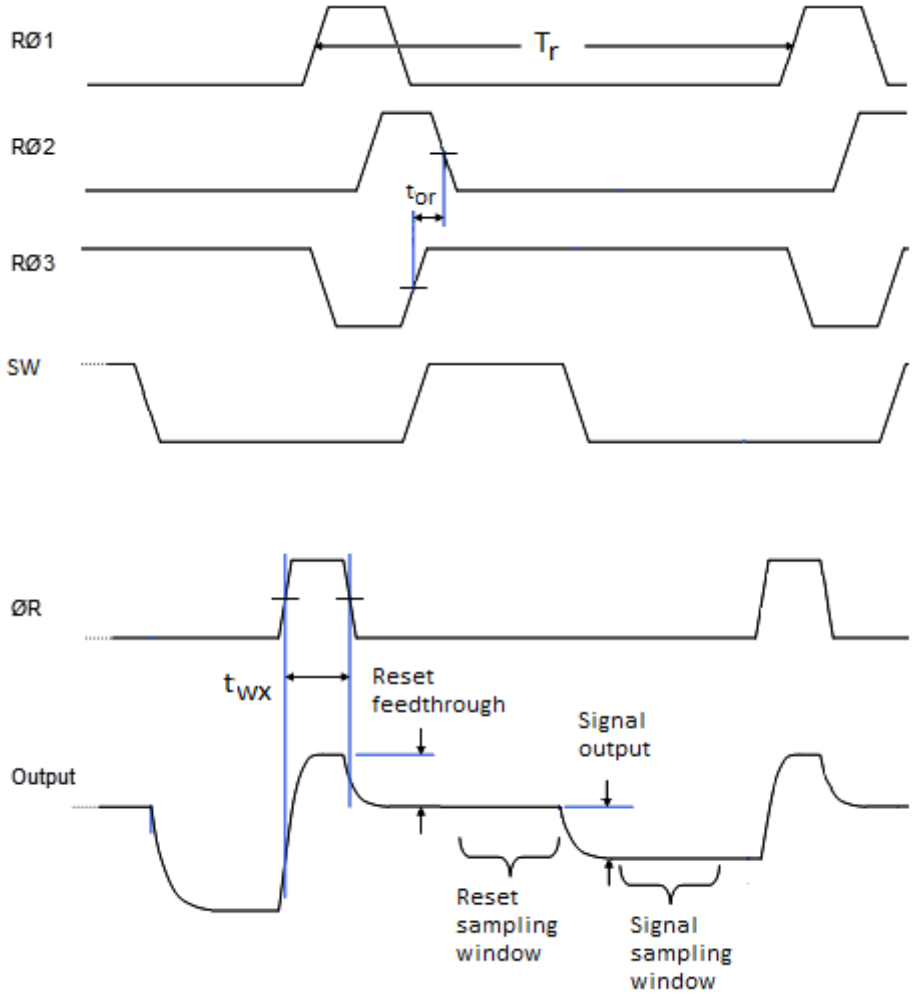
FRAME READOUT TIMING DIAGRAM



DETAIL OF LINE TRANSFER (Not to scale)



DETAIL OF OUTPUT CLOCKING

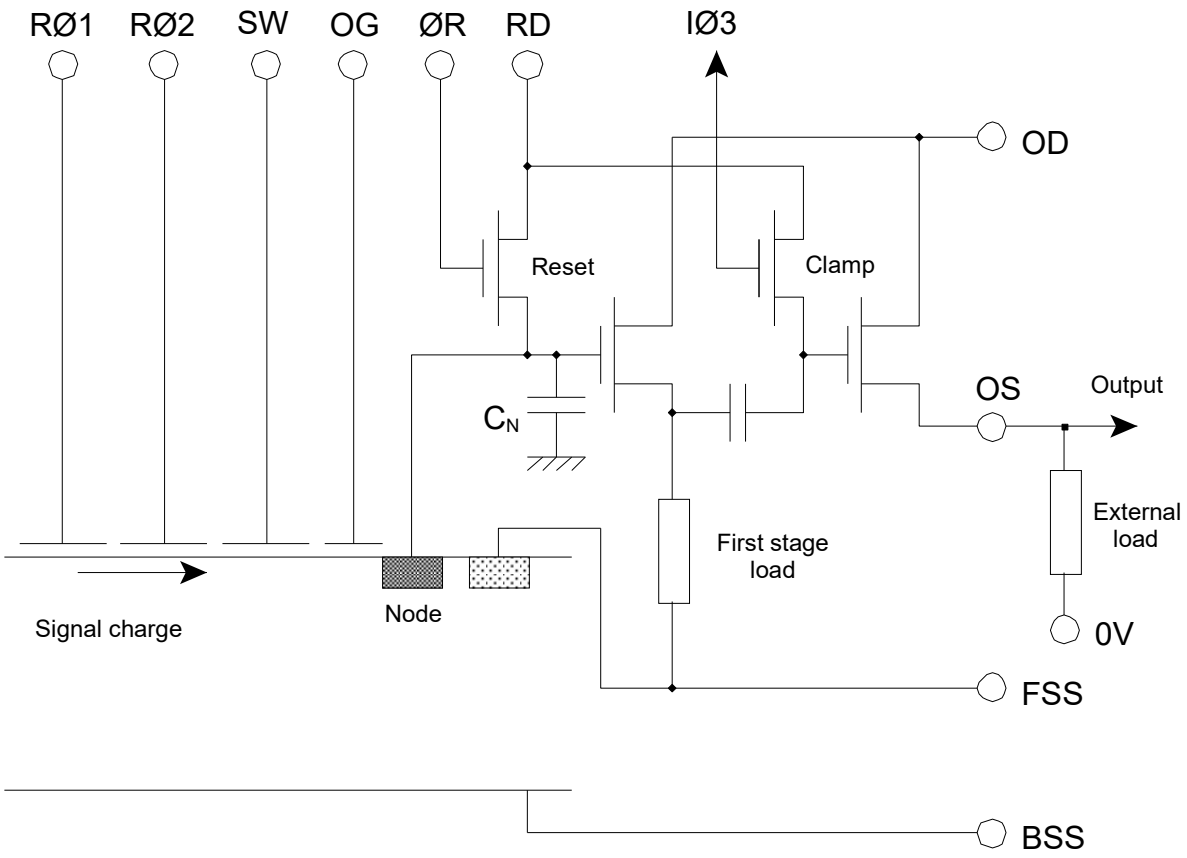


CLOCK TIMING REQUIREMENTS

Symbol	Description	Min	Typ	Max	Unit
T_p	Image clock period	3000	3250	Note 15	µs
T_i	Line transfer Time	-	4510	Note 15	µs
t_{wi}	Image clock pulse width	1500	1800	Note 15	µs
t_{oi}	Image clock pulse overlap	400	500	-	µs
t_{li}	Image clock pulse, two phase low	400	500	Note 15	µs
t_{dir}	Delay time, IØ stop to RØ start	5	20	Note 15	µs
t_{dri}	Delay time, RØ stop to IØ start	5	20	Note 15	µs
T_r	Output register clock cycle period	1	2	Note 16	µs
t_{rr}	Register pulse rise time (10 to 90%)	50	90	Note 17	ns
t_{fr}	Register pulse fall time (10 to 90%)	50	90	Note 17-	ns
t_{or}	Register pulse overlap (50%)	20	120	Note 17-	ns
t_{wx}	Reset pulse width	30	170	Note 17-	ns
t_{rx}	Reset pulse rise and fall times	20	80	Note 17-	ns
t_{dx}	Delay time, ØR low to RØ3 low	-	80	Note 17-	ns

15) No maximum other than that necessary to achieve an acceptable dark signal at longer readout times and general compliance to the line transfer timing diagram. Scale to T_p.
16) Determined by readout time requirement.
17) Scale to T_r.

OUTPUT CIRCUIT

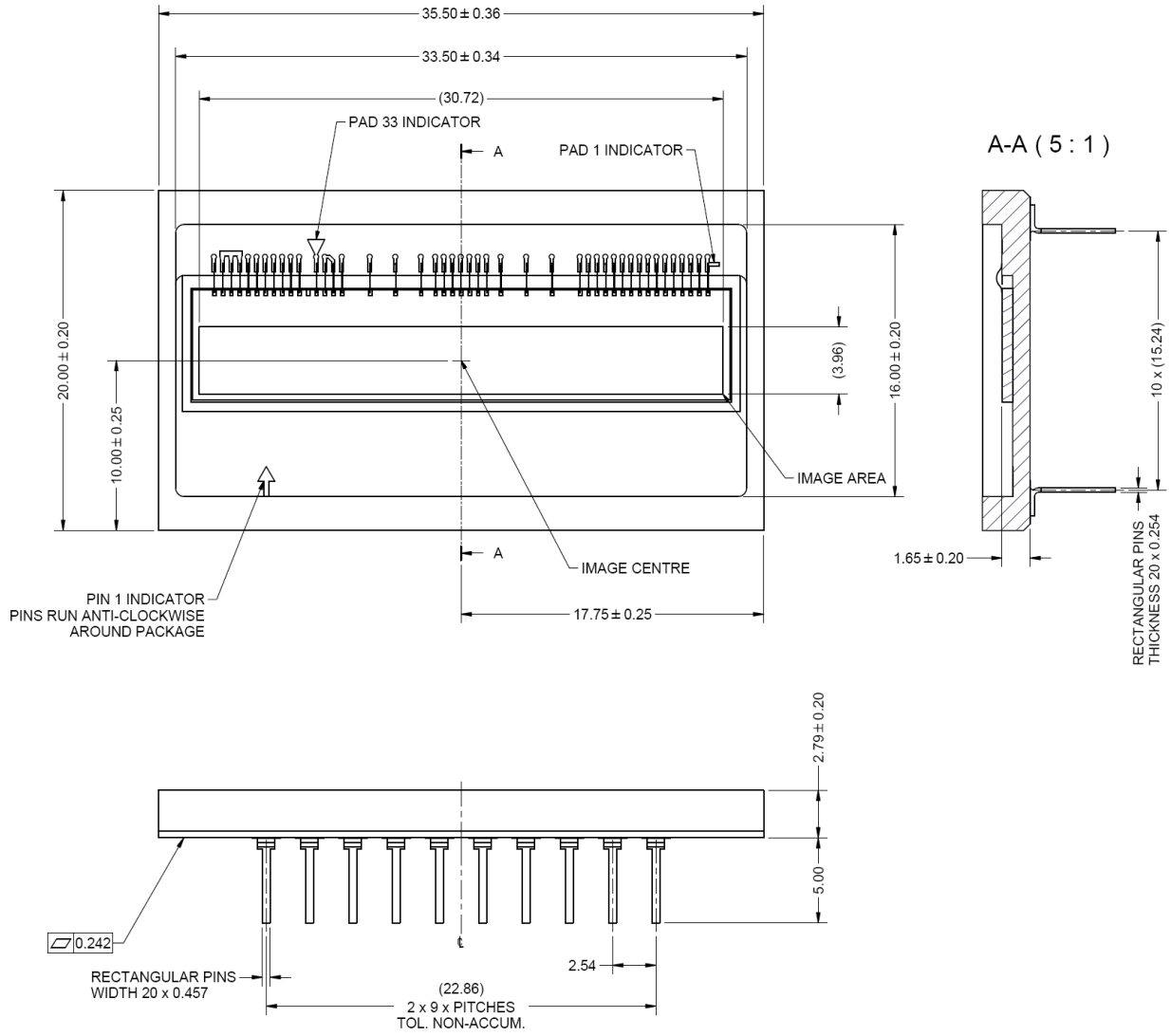


NOTES

18) The amplifier has a DC restoration circuit, which is activated internally whenever IØ3 is pulsed high.

PACKAGE

(All dimensions are nominal and are in mm)

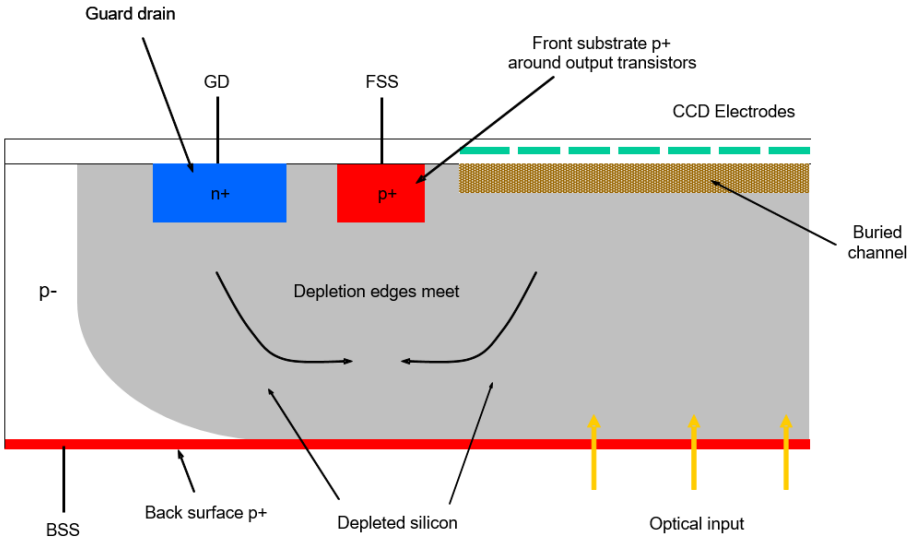


DEEP DEPLETED AIMO DEVICE TECHNOLOGY

Extending the long wavelength response of back-face devices requires the use of thicker silicon, but this must be fully depleted to avoid loss of spatial resolution through sideways diffusion of charge. The depth of depletion is proportional to square root of the operating voltages and the silicon resistivity, but there is a practical limit to both and possibilities for maintaining full-depletion with increasing thickness are therefore limited.

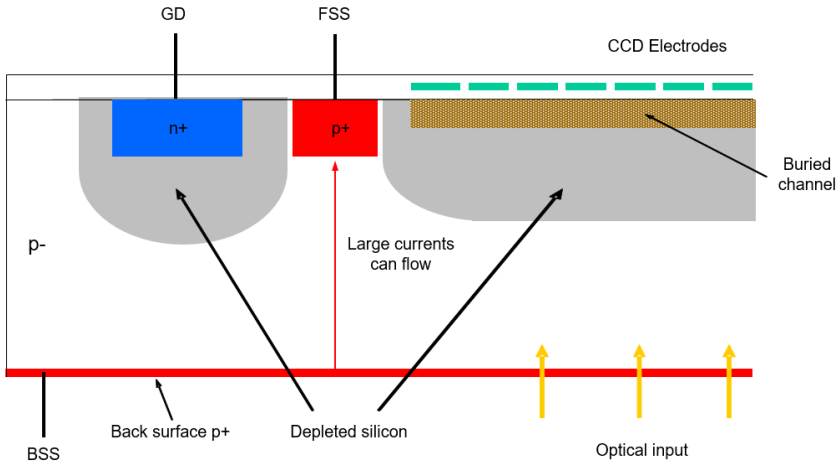
In standard devices the bulk of the silicon substrate is all at the same bias voltage V_{SS}. It is possible to take V_{SS} to negative voltages to increase depletion, but the limit is generally set by the onset of avalanche breakdown in the p-n junctions of the output circuit components. For AIMO devices the high positive substrate voltage required to achieve surface potential pinning and reduce dark signal further reduces the achievable depletion depth.

The use of a lower or negative substrate bias on the back of the silicon V_{BSS} to increase the depth of depletion under the electrodes, whilst still maintaining a bias on the front-surface of the silicon V_{FSS} at a voltage level normally used for V_{SS} allows the output circuits to function normally and pinning to be maintained. However, for this to be possible, current flow between the front and back bias connections must be avoided. This is achieved using an additional “guard drain” diode at bias V_{GD}, as shown below.



With correct bias conditions the depletion regions from the CCD channel and the guard diode merge to block the conductive path, rather like the operation of a JFET, as shown above. If incorrect, then there is a direct resistive path between the front and back contacts and excessive currents can flow, as shown below.

It is therefore important to use the specified bias levels and the switch-on and switch-off sequences.



ORDERING INFORMATION

CCD261-04-g-xxx
g = cosmetic grade
xxx= specific variant type (e.g. thickness and coating)

CCD261-04-g-S31: Deep Depleted Silicon, NIR AR coating

For further information on the performance of this and other options, please contact Teledyne e2v.

HANDLING CCD SENSORS

CCD sensors, in common with most high performance MOS IC devices, are static sensitive. In certain cases a discharge of static electricity may destroy or irreversibly degrade the device. Accordingly, full antistatic handling precautions should be taken whenever using a CCD sensor or module. These include:-

- Working at a fully grounded workbench
- Operator wearing a grounded wrist strap
- All receiving socket pins to be positively grounded
- Unattended CCDs should not be left out of their conducting foam or socket.

Evidence of incorrect handling will invalidate the warranty.

HIGH ENERGY RADIATION

Device characteristics will change when subject to ionising radiation.
Users planning to operate CCDs in high radiation environments are advised to contact Teledyne e2v.

TEMPERATURE LIMITS

	Min	Typical	Max	
Storage	148	-	323	K
Operating	223	263	293	K

Operation or storage in humid conditions may give rise to ice on the sensor surface on cooling, causing irreversible damage.

Maximum device heating/cooling ..... 5 K/min