TELEDYNE e2v
Everywhereyoulook™
Part of the Teledyne Imaging Group

QUANTUM TIME & FREQUENCY SOLUTIONS

Teledyne Chip Scale Atomic Clock

The **Teledyne Chip Scale Atomic Clock (TCSAC)** is ideal for applications where a clock with high accuracy, high stability, and low power consumption is needed. The TCSAC provides these characteristics at an affordable price. Teledyne e2v has a long history of providing technology-based components and systems for use in complex applications.

The TCSAC is designed with a configurable output frequency to meet your particular application requirements. The unit will also accept an external 1 PPS signal to discipline its frequency and the phase of its 1 PPS output.

An RS-232 serial interface is available to monitor and control the unit. The interface also allows the TCSAC internal time of day to be set and interpreted.

KEY FEATURES (Preliminary)

- Configurable Output Frequency
- RS-232 Interface for Monitoring and Control
- Short Term Stability (Allan Deviation) of 3E-10 @ TAU = 1 sec
- RF Output Phase Noise (SSB) < -58 dBc/Hz @ 1 Hz
- Aging < 3E–10/month
- Volume < 23 cc, 1.6" x 1.39" x 0.628"
- Power Requirement < 180 mW

APPLICATIONS

- Banking/Financial Markets
- C4I, Tactical Communications/ECM and Soldier Systems
- Critical National Infrastructure (CNI) Protection
- Energy and Transport Infrastructure
- Fixed and Mobile Communications Networks (including 5G)
- GPS Challenged Environments and Autonomous Systems
- Sensor Networks
- Undersea Seismic Sensing and Scientific Applications

Teledyne CSAC Preliminary Data Sheet Specifications

Specification RF Output	
Frequency	10 MHz, 16.384 MHz
Format	LVCMOS
Amplitude	0 V to 3.3 V
Load impedance	1 MΩ
Number of outputs	1

1 PPS Output	
Rise time	< 5 ns
Pulse width	1-200 µs (programmable)
Logic low max (Vol)	< 0.5 V
Logic high min (Voh)	> 2.5 V
Load impedance	1 MΩ
Number of outputs	1

1 PPS Input	
Format	Rising edge
Logic low max (Vol)	< 0.5 V
Logic high min (Voh)	≥ 2.4 V and < 3.3 V
Input impedance	100 kΩ
Number of inputs	1

Serial Communication	
Protocol	RS-232
Format	LVCMOS, 0 V to 3.3 V
TX/RX impedance	100 kΩ
Baud rate	38,400

Built-In Test Equipment (BITE) Output	
Format	LVCMOS, 0 V to 3.3 V
Load impedance	100 kΩ
Logic	0 = Normal operation; 1 = Alarm

Input Power	
Input voltage (Vcc)	3.3 VDC; Range from 3.2 to 3.6 VDC
Operating	< 180 mW
Warm-up	< 205 mW

Dimensions (H x W x D)
0.628" x 1.6" x 1.39"

Weight
42.6 g

MTBF
TBD

Operating Characteristics	
Operating temperature	–10°C to +60°C
Temperature coefficient	< 5 x 10^{-10}

PIN NO.	I.D.		
1	Tune	7	Vcc
2	N/A	8	GND
3	N/A	9	1 PPS IN
4	BITE	10	1 PPS OUT
5	Tx	11	N/A
6	Rx	12	RF OUT

Operating Characteristics (continued)	
Frequency change over allowable input voltage range	± 4 x 10^{-10}
Magnetic sensitivity (≤ 2.0 Gauss)	± 9 x 10^{-11}/Gauss
Radiated emissions	Compliant to FCC part 15, Class B, when mounted properly onto host PCB
Vibration	Maintains lock under MIL-STD-810G, method 514.6, annex E, 7.7 grms
Humidity	0 to 95% RH per MIL-STD-810G, method 507.5 procedure II

Storage and Transport Characteristics (non-operating)	
Storage temperature	–55°C to +85°C
Shock (1 ms half-sine)	750 g

Allan Deviation	
Tau = 1 sec	3 x 10^{-10}
Tau = 10 sec	1 x 10^{-10}
Tau = 100 sec	3 x 10^{-11}
Tau = 1000 sec	1 x 10^{-11} (typical)

RF Output Phase Noise (SSB)	
1 Hz	< –58 dBc/Hz
10 Hz	< –85 dBc/Hz
100 Hz	< –113 dBc/Hz
1000 Hz	< –130 dBc/Hz
10,000 Hz	< –140 dBc/Hz
100,000 Hz	< –142 dBc/Hz

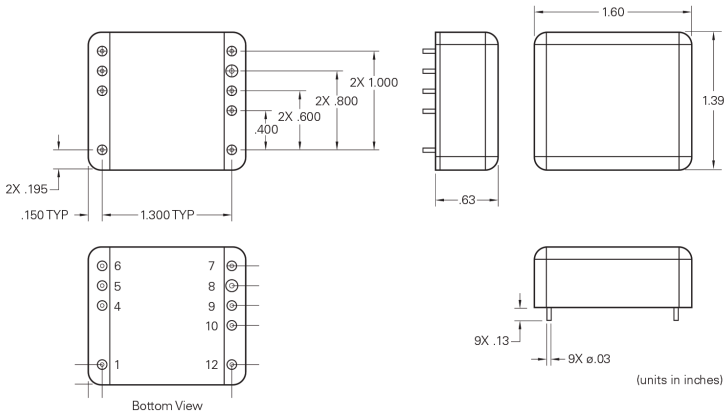
Frequency Accuracy	
Max offset at shipment	± 5 x 10^{-11}
Max retrace (48 hrs. off)	± 3 x 10^{-10} (TBD)
Aging, monthly	< 3 x 10^{-10}
Aging, yearly	< 2 x 10^{-9}
1 PPS sync	± 100 ns

Digital Tuning	
Range	± 4 x 10^{-8}
Resolution	1.3 x 10^{-12} (10 MHz); 1.5 x 10^{-12} (16.384 MHz)

Analog Tuning	
Range	± 2.5 x 10^{-9}
Resolution	1.3 x 10^{-12} (10 MHz); 1.5 x 10^{-12} (16.384 MHz)
Input	0-2.5V into 100 kΩ

Warm-up Time
TBD

Soldering Instructions
TBD



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